Notice of Allowability	Application No.	Applicant(s)	
	10/662,607	FARRENKOPF, DOUGLAS ROBERT	
	Examiner	Art Unit	
	Ronald W. Leja	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment of 5/19/2005*.

2. ☒ The allowed claim(s) is/are *16-27*.

3. ☒ The drawings filed on *29 September 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Ronald W. Leja
Primary Examiner
Art Unit 2836

5/30/05

The following is an Examiner's Statement of Reasons for Allowance: It is the position of the Examiner that the ESD Preamble language, in Independent Claims 16 and 22, be given patentable weight; "ESD protection", ties in the body language, "to-be-protected circuit", thereby rendering meaning and understanding to the overall claim language with the specifically connected npn transistor and MOS transistor. It is noted that the ESD protection Art is considered to be a very narrow and crowded Art, wherein small changes lend themselves to being considered novel and unobvious. This is the case with the instant Claims 16-27. Chang (6,400,540) is very close art, but does not disclose, mention or suggest the use of a npn transistor for (B3). Chang discloses that it is known to utilize or replace a transistor with another type, i.e. Col. 3, lines 55-65 and in replacement of (P1) in Fig. 5 with (N51) in Fig. 6. Often changing the conductivity type of a control transistor often requires changing the conductivity type of the controlled transistor (i.e. B53). It should be pointed-out that the Examiner is well aware that it is well known in the Art and known that it is well within the abilities of one having ordinary skill in the Art to change conductivity types of transistors. However, it is the position of the Examiner, that the motivation for doing such a conductivity change is not always apparent or obvious. There does not appear to be strong motivation for making changes to transistor (B3) in Chang so as to be an n-p-n transistor. Figure 4 of Sellnau et al. (6,204,715) illustrates the connections of the npn and MOS transistors with respect to the pad and GND, but the

circuit is not for ESD protection, but rather for sensor amplification. One would not be motivated to pick this circuit out of Sellnau et al. and utilize it for ESD protection of a "to-be-protected circuit" connected to the pad. Ohannes et al. (5,521,789) teach the use of the two required transistors, but do not teach the specific connections of the collector to the pad and the emitter to ground. There does not appear to be strong motivation to change the circuit of Ohannes et al. (delete the diode and connect the collector to the pad and the emitter to ground) with the exception of hind-sight. Kitagawa (US 2003/0214773) illustrates another example wherein the drain of the MOS transistor is shown connected to the base of the npn transistor, but the collector of the npn transistor is not connected to the pad. In fact, the npn transistor is connected to the pad through the pnp transistor which together form a different device, namely an SCR. One could make the argument that the npn transistor is connected to the pad, via transistor (Q5), however, this position leads to an unreasonable interpretation i.e., wherein every component within a device is connected to every other component within the device. The crowded ESD protection Art does not lend itself to such interpretations. For example, in Holberg et al. (6,285,536), there is disclosed (Fig. 5) a MOS transistor (505) having its drain connected to the base of npn transistor (506) and the emitter of transistor (506) is connected to ground; the circuit helps protect the amplifier (133) from spikes. However, the collector is not disclosed as being connected to the pad (100). If one wanted to interpret that the

collector was connected to pad (100) (via elements 132 and 99), then the drain of MOS transistor (105) would also have to be considered connected to the base of npn transistor (506) and this fact does not meet the claim language of "only a single drain being connected to the base". Therefore, it is the opinion of the Examiner, that there does not appear to be strong motivation for modifying Figure 5 of Holberg et al., (i.e. making the collector of npn transistor 506 to be connected to the pad 100 for ESD protection of the circuit), since additionally, element EDPS (99) is already taught as being the ESD protection connected to the pad (100) for the circuit. Independent Claims 16 and 22 are considered novel and unobvious in view of the Prior Art of Record.

Any comments considered necessary by Applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ronald W. Leja whose telephone number is (571)272-2053. The examiner can normally be reached on Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)272-2800. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ronald W Leja
Primary Examiner
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5/30/05

rwl
May 29, 2005